

**CIRCUIT FOR GENERATING CLOCK SIGNAL AND DECODING DATA
SIGNAL FOR USE IN CONTACTLESS INTEGRATED CIRCUIT CARD**

ABSTRACT OF THE DISCLOSURE

An integrated circuit card which includes a circuit for generating a
5 clock signal and for restoring data. The circuit includes a receiver for
receiving a radio frequency signal having a pause period; a divider for
dividing the received signal; a first counter for counting a period of the
divided signal at each non-pause period of the received signal; a second
counter for counting a period of the divided signal; and a decoder for
10 generating a synchronous clock signal and a decoded data signal in response to
outputs of the first and second counters. The second counter is reset by the
synchronous clock signal. The circuit is capable of generating a synchronous
clock signal and decoding a received data signal so as to be compatible with
ISO/IEC 14443 Type A protocol, based on the received radio frequency signal
15 that is transferred from a card reader. The circuit provides an exact decoding
result even when the pause period of the radio frequency received from the
card reader varies over a predetermined range.